It should be noted that three criteria must be met to establish a prima facie case of obviousness. *M.P.E.P. § 2143*. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings to achieve the claimed invention. *Id.* Second, there must be a reasonable expectation of success. *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). Third, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

The present invention is related to a display device and one of the features of the invention is that the device comprises: a semiconductor film comprising a plurality of channel forming regions, a plurality of impurity regions (i.e. low concentration impurity regions and a high concentration impurity region), a source region, and a drain region; and a gate electrode overlapping with the channel forming regions and some of the impurity regions, with a gate insulating film interposed therebetween, wherein said some of the impurity regions are located between the plurality of channel regions in the semiconductor film as shown in Figs. 4C, 6D, and 9. In order to clarify the above feature, claims 1-4, 6-9, 15, 16, 18 and 19 have been amended and new claims 21-42 have been added.

In the Office Action, the examiner asserts that Yudasaka et al. disclose a display device having a pixel portion and a driver circuit portion on the same substrate wherein an active layer of a pixel TFT has a low concentration impurity regions, a channel forming region, and a high concentration impurity region between source and drain regions. The Examiner concedes that Yudasaka "does not disclose that said low concentration impurity region partially overlaps with said gate electrode with a gate insulating film interposed therebetween" (paragraph 2 of Paper No. 8). Kobayashi is cited by the Examiner to show this feature.

The Applicants respectfully contend that the Office Action has failed to set forth a *prima facie* case of obviousness. The Examiner has not given any indication that one with ordinary skill in the art at the time of the invention would have had a reasonable expectation of success when combining Yudasaka and Kobayashi.

Furthermore, the prior art does not teach or suggest all the claim limitations. Kobayashi does not correct the deficiencies in Yudasaka. The Examiner cites Kobayshi in order to teach the overlapping described above. However, it should be noted that both Yudasaka and Kobayashi fail to teach that a semiconductor film comprises a plurality of channel forming regions and a

plurality of impurity regions, wherein some impurity regions are located between the plurality of the channel forming regions in the semiconductor film. Accordingly, even if motivation to combine Yudasaka and Kobayashi were found and one with ordinary skill in the art at the time of the invention had a reasonable expectation of success, Applicants believe that it is not possible to obtain the claimed invention.

The Applicants further contend that even assuming, *arguendo*, that the combination of Yudasaka and Kobayashi is proper, there is a lack of suggestion as to why a skilled artisan would use the proposed modifications to achieve the unobvious advantages first recognized by the Applicants. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990).

The Examiner further argues that claims 2 and 7 are obvious in view of teachings in Yudasaka and that claims 5, 10, 17 and 20 are obvious in view of teachings noted by Official Notice. For the reasons stated above, Applicants contend that the Examiner has failed to make a *prima facie* case of obviousness. The features noted by the Examiner in Yudasaka and by means of Official Notice do not cure the deficiencies in Yudasaka and Kobayashi.

Therefore, Applicants respectfully request that the Examiner withdraw the § 103 rejections.

Claims 3, 4, 8, 9, 16, and 19 are Held Allowable

The Examiner is thanked for indicating the allowability of claims 3, 4, 8, 9, 16 and 19.

New Claims 21-42 are Allowable

New claims 21-42 have been added to better claim the invention, of which only claim 35 is independent. Claim 35 is similar in structure to claim 1, and for the reasons stated above, should be held allowable. Claims 21-34, and 36-42 should be held allowable as dependent on allowable subject matter.

Conclusion

Prompt and favorable consideration is requested. In view of the above, all the claims in this case are believed to be in condition for allowance. Should the Examiner deem that any

further action by the Applicant would be desirable in placing this application in even better condition for issue, he is requested to contact the undersigned.

Respectfully submitted,

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The Commissioner is hereby authorized to charge any fees connected with this filing which may be required now, or credit any overpayment to Deposit Account No. 19-2380.

Respectfully submitted,

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MARKED-UP VERSION OF THE AMENDED CLAIMS

1. (Amended) A display device [having] comprising a pixel portion and a driver circuit portion on [the same] a substrate, said pixel portion comprising:

[wherein an active layer of a pixel TFT formed in said pixel portion has a low concentration impurity region, a channel forming region, and a high concentration impurity region which are formed between a source region and a drain region,

wherein said channel forming region and said high concentration impurity region are formed under a gate electrode, and

wherein said low concentration impurity region partially overlaps with said gate electrode with a gate insulating film interposed therebetween]

a semiconductor film comprising a plurality of channel forming regions, a plurality of impurity regions, a source region, and a drain region; and

a gate electrode overlapping with the channel forming regions and some of the impurity regions, with a gate insulating film interposed therebetween,

wherein said some of the impurity regions are located between the plurality of channel regions in the semiconductor film.

2. (Amended) A device according to claim 1, wherein at least two of said [low concentration] impurity regions overlapped with the gate electrode contain[s] an element [that belongs to group XV in the periodic table] at a concentration of 2×10^{16} to 5×10^{19} atoms/cm^3, and at least one of the [said high concentration] impurity regions overlapped with the gate electrode contain[s] the element at a concentration of 5×10^{19} to 3×10^{21} atoms/cm^3.

3. (Amended) A device according to claim 1, wherein a thickness of [the] a gate insulating film of a TFT in said driver circuit portion is thinner than that of the gate insulating film of [the pixel] a TFT in the pixel portion.

4. (Amended) A device according to claim 1, wherein [the] a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness.

6. (Amended) A display device [having] comprising a pixel portion and a driver circuit portion on [the same] a substrate, said pixel portion comprising:

[wherein an active layer of a pixel TFT formed in said pixel portion has a low concentration impurity region, a channel forming region, and a high concentration impurity region which are formed between a source region and a drain region,

wherein said channel forming region and said high concentration impurity region are formed under a gate electrode, and

wherein said low concentration impurity region has a region that overlaps with said gate electrode with a gate insulating film interposed therebetween, and a region that does not overlap with the gate electrode]

a semiconductor film comprising a plurality of channel forming regions, a plurality of low concentration impurity regions, a high concentration impurity region, a source region, and a drain region; and

a gate electrode overlapping with the channel forming regions, some of the low concentration impurity regions, and the high concentration impurity region, with a gate insulating film interposed therebetween,

wherein said some of the low concentration impurity regions and the high concentration impurity region are located between the plurality of the channel regions in the semiconductor film.

7. (Amended) A device according to claim 6, wherein each of said low concentration impurity regions contains an element [that belongs to group XV in the periodic table] at a concentration of 2×10^{16} to 5×10^{19} atoms/cm^3, and said high concentration impurity region contains the element at a concentration of 5×10^{19} to 3×10^{21} atoms/cm^3.

8. (Amended) A device according to claim 6, wherein a thickness of [the] a gate insulating film of a TFT in said driver circuit portion is thinner than that of the gate insulating film of [the pixel] a TFT in said pixel portion.

9. (Amended) A device according to claim 6, wherein [the] a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness.

15. (Amended) A display device [having] comprising a pixel portion and a driver circuit portion on a substrate, said pixel portion comprising:

a semiconductor film [having] comprising at least two channel forming regions, [low concentration] at least one first impurity region[s], at least one second impurity region, a source region, and a drain region; and

a gate electrode [over at least over] overlapped with said two channel forming regions and the first impurity region, and a part of the second impurity region with a gate insulating film interposed therebetween,

wherein [the low concentration impurity regions include a region that overlaps with the gate electrode] one of the channel forming regions is located between the first impurity region and the second impurity region.

16. (Amended) A device according to claim 15, wherein a thickness of [the] a gate insulating film of a thin film transistor in said driver circuit portion is thinner than that of the gate insulating film in the pixel portion.

18. (Amended) A display device [having] comprising a pixel portion and a driver circuit portion on a substrate, said pixel portion comprising:

a semiconductor film having at least two channel forming regions, [high concentration impurity regions formed between the channel forming regions,] first and second low concentration impurity regions, high concentration impurity regions, a source region, and a drain region; and

a gate electrode [over at least over] overlapping with said two channel forming regions, the first low concentration impurity regions, the high concentration impurity region, and portions of the second impurity regions, with a gate insulating film interposed therebetween,

wherein the [low concentration impurity region[s include a region that overlaps with the gate electrode] high concentration impurity region is located between the channel forming regions.

19. (Amended) A device according to claim 18, wherein a thickness of [the] a gate insulating film of a thin film transistor in said driver circuit portion is thinner than that of the gate insulating film in the pixel portion.